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# INTERNALLY MATCHED ( IM ) PLATED SOURCE BRIDGE ( PSB ) POWER GaAs FET ACHIEVING A HIGH PERFORMANCE POWER AMPLIFIER IN X-BAND

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ABSTRACT

Internal matched devices with 2W and 5W power output at 10 GHz have been developed by using up-side-down mounted GaAs FETs which have PSB ( Plated Source Bridge ) structures.
By parallel running two 5W devices, 7W solid-state power amplifiers in X-band have been practical.

## Introduction

In these days, in order to decrease size and weight of an equipment and further improve reliability, replacing a TWT amplifier by a solid-state amplifier using a power GaAs FET is strongly demanded in above X band. A power FET with a high performance over a broad band is required in a high frequency of above X band, which makes possible providing a solid-state amplifier.

In frequencies less than X band, a 5W GaAs FET which an up-side-up type FET chip is mounted is commercially available. As lead inductance of such kind of FET is larger than the one of an up-side-down type FET, it is difficult to have a good performance in frequencies above X band.[1]

Taking these into consideration, authors have developed an internally matched ( IM ) plated source bridge ( PSB ) power GaAs FET with a high performance in X band.[2]
Technology for mounting a FET chip up-side-down and for internally matching the input and output impedance to 50Ω has been established. Using the technology, $P_{1dB}$ more than 2W with $G_{LP}$ of 7 dB and $P_{1dB}$ more than 5W with $G_{LP}$ of 5 dB have been reproductively obtained in 9 to 10 GHz.

It is confirmed that only by cascading these devices and parallel running, a high power and broad band solid-state amplifier can be constructed in the corresponding frequencies.

## Design of IM Power GaAs FETs for High Frequencies

In order to improve power and gain at a high frequency, it is indispensable to minimize factors introduced by thermal problems and at a high frequency as much as possible.

For obtaining high gain at a high frequency, decrease of parasitics and increase of transfer conductance and minimizing a lead inductance are important and for high power, decrease of thermal resistance and increase of breakdown voltage.

This consideration should be reflected on designing a device. For a practical design, the configurational and structural parameters of GaAs FET chips are need to be optimized, since these parameters are often competitive.

Main improvements are as follows,

(1) Optimization of the unit gate length and the spacing between electrodes
(2) Deep recess structure
(3) Thickness of gate electrode
(4) Selection of a high quality semi-insulating GaAs substrate having a high thermal stability
(5) Formation of high quality buffer layer with a small impurity density and active layer with proper carrier profile[3]
(6) PSB structure
(7) Up-side-down mounting structure.

Since the total gate width is very large in the case of high power GaAs FETs, the impedance of GaAs FET chips becomes so low that input and output impedances are affected by parasitic capacitance and inductance of a package. It is difficult to make matching circuits out of a package, especially in high frequencies.
Fig. 1 shows the cross-sectional illustration of internally matched device mounting a FET chip up-side-down. Input and output impedances were matched to 50Ω by the lumped element circuits consisting of C (capatitance) and L (inductance).
C were formed on high dielectric substrates and L were realized by bonding Au wires between C patterns on the substrates.

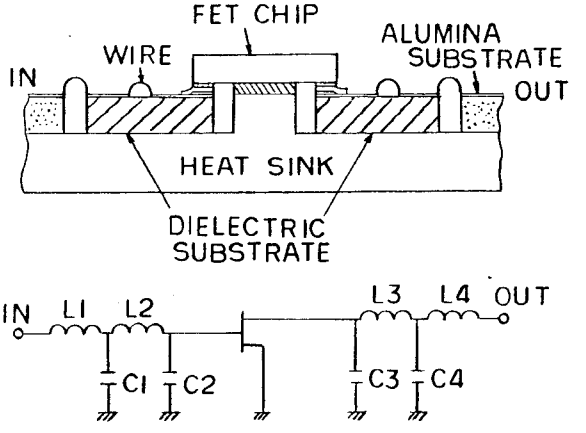


Fig. 1
Cross-sectional diagram and equivalent circuit for internally matched circuit.


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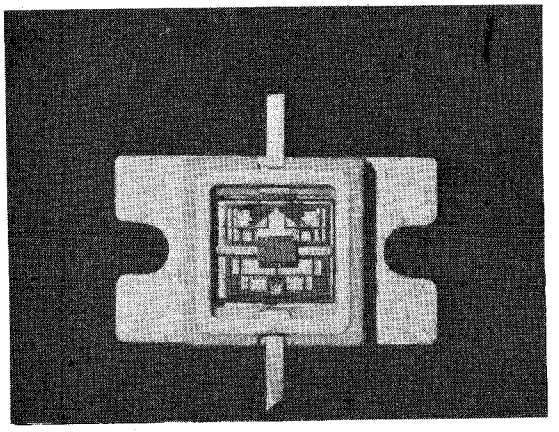
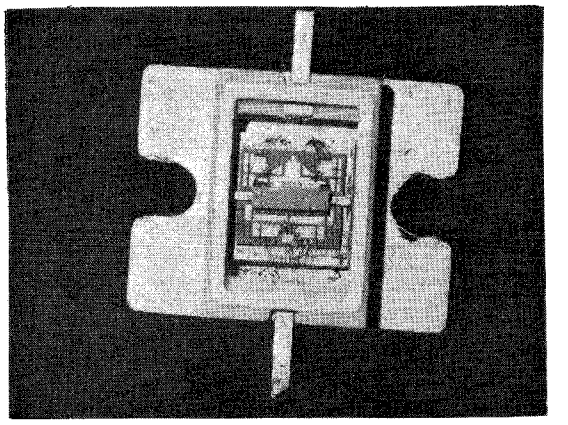


2 W FET



5 W FET

Fig. 2 Inside pictures of internally matched 2 W and 5 W FETs.

## Fabrication

Fig. 2 shows the inside views of internally matched power GaAs FETs with 2 W and 5 W mounted up-side-down. N type GaAs epitaxial wafers having carrier concentration of 1.2 to 1.5 X $10^{17}$ $cm^{-3}$ were used. The gate electrodes were formed by Al and had 0.8 $\mu$m gate length, 200 $\mu$m unit gate width. Total gate width was 7200 $\mu$m for a 2 W FET and 21600 $\mu$m ( 10800 $\mu$m X 2 chips ) for a 5 W FET. Source and drain electrodes were made by Au-Ge/Ni metallization. The spacing between them was 4 $\mu$m.

The PSB source electrode was directly connected to the package by Au-Ge solder. The gate and drain electrodes were directly connected to the dielectric substrates by Au ribbons. Matching of internal circuits to 50 $\Omega$ was carried out by fine adjustment with VSWR of less than 2.5.

## Electrical Characteristics

Fig. 3 shows $P_{1dB}$ and $G_{LP}$ dependence on frequencies both for 2 W and 5 W FETs. $P_{1dB}$ and $G_{LP}$ more than 2 W and 7 dB for 2 W FETs , 4 W and 5 dB for 5 W FETs were obtained in 9 to 10 GHz. These characteristics have been reproductively got.

Fig. 4 shows the amplifier characteristics obtained by simple cascade connection of a 2 W FET and a 5 W FET as shown by the inserted figure.

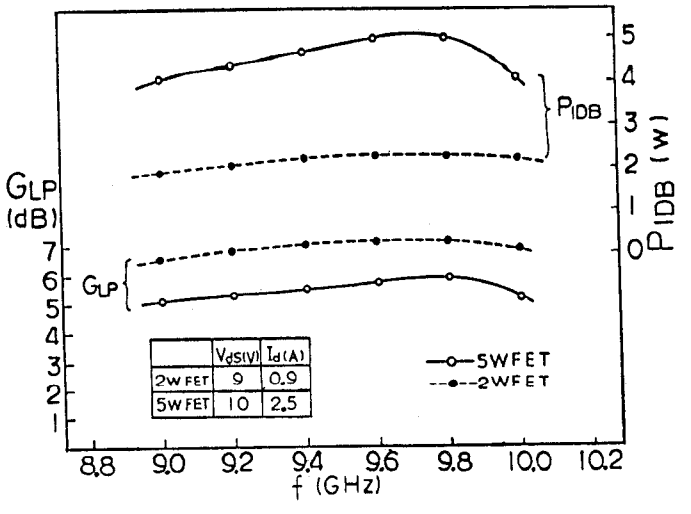



Fig. 3 $P_{1dB}$ and $G_{LP}$ as a function of frequencies both for 2 W and 5 W FETs.

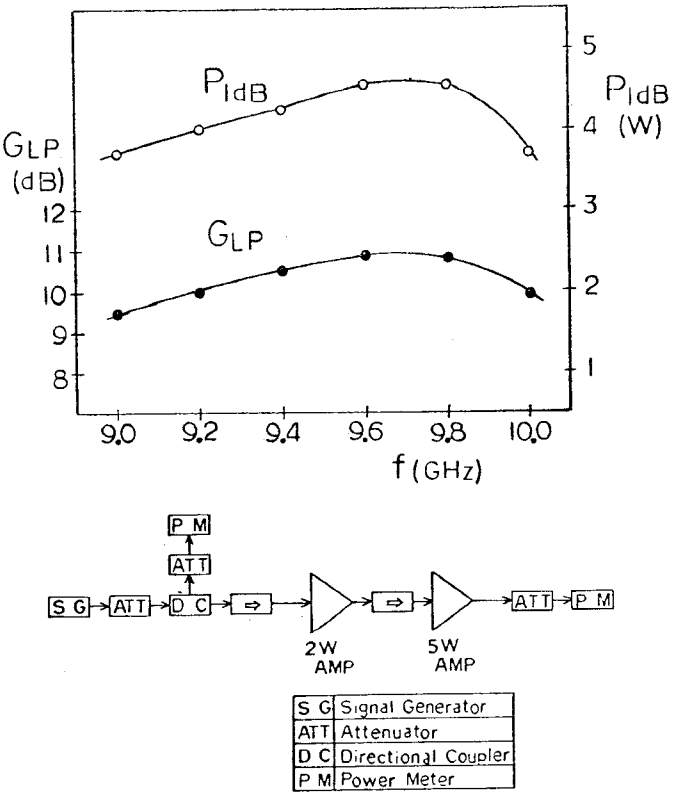



Fig. 4 Amplifier's characteristics obtained by cascade connection of 2 W and 5 W FETs.

A solid-state amplifier in X band has become practical only by installing a circulator between FETs without any outside matching circuit.

By parallel running two 5 W FETs as shown in Fig.5 , 7 W amplifier has been also achieved.
This amplifier's characteristics were $P_{1dB}$=7 W and $G_{LP}$=5.8 dB as shown in Fig. 6.

## Conclusion

Internally matched 2 W and 5 W power PSB GaAs FETs at X band have been developed.
By optimizing the configuration and the structure of FET chip, selecting a high quality epitaxial wafer, mounting a FET chip up-side-down and then optimizing internal match circuits, high performance devices have been reproductively fabricated.

4 W broad band solid-state amplifiers and 7 W amplifiers in X band become practical only by cascade connection and further parallel connection of these developed FETs.

Here developed devices are believed to contribute to further promote replacing conventional TWT power amplifiers with solid-state amplifiers.


## Acknowledgement

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## References


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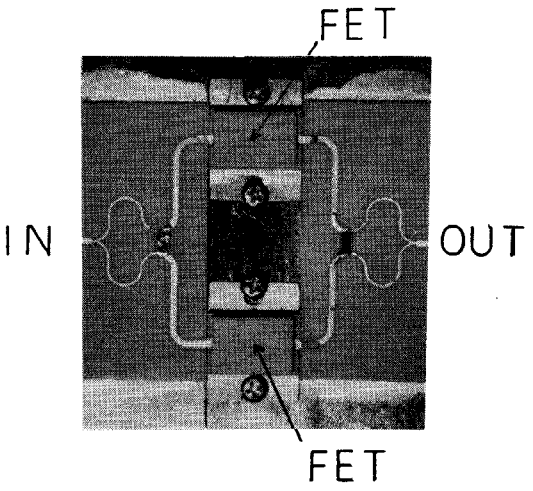


Fig. 5 Circuit for parallel running two 5 W FETs

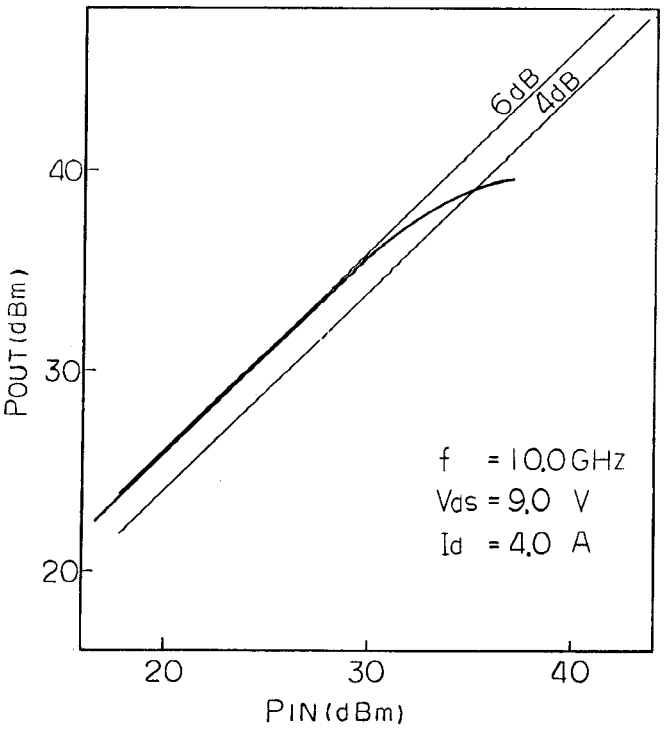


Fig. 6 7 W amplifier's characteristics